Report on Hardware Meeting Held 23rd February 2005 during GSI AGATA week

The main task of the meeting was to identify the people who will work to refine the interfaces between the different parts of the AGATA hardware. Most of these interfaces are partially defined- the electrical (or fibre) interfaces are known, but the protocols to be operated over them have not been discussed or agreed by people representing the teams at both ends of the link. The design process will soon require that FPGAs are programmed and so these protocols must be agreed so that FPGA design can proceed unhindered. The full definitions, including protocol agreements, will be discussed and then recorded in either new documents (which will later become chapters in the appropriate specifications when completed) or by updating interfaces defined in existing specifications.

Algorithm for digitiser input offset adjustments.
As yet only one digital algorithm exists for offset adjustment (University of Milan- see Alberto Pullia's presentation in Padova, December 2004). This algorithm has yet to be tested. It works at high rate (sample by sample) so would need to be implemented in the digitiser. It has the capacity to generate extra data bits, extending the effective width of the sampling ADCs beyond 14 bits by adjusting the offset. In this case the link from digitiser to pre-processor would either need more bits (data width), or a new slow control protocol which, for example, selects the 14 MSBs from the available data and puts them into the 14 available data transmission bits.

No-one volunteered to develop any other (slower) algorithm to operate in the pre-processor. In the following plenary session **it was agreed** that the demonstrator can start without this algorithm as long as the system contains the connections (hardware and protocol) to add it later either in the pre-processing or the digitiser.

Protocol for digitiser input offset adjustments (from pre-processing)
Sebastien Lhenoret and Patrick Coleman-Smith will discuss and propose this protocol. Patrick suggested that we use the 6 spare optical lines from digitiser to pre-processor to reply to (handshake with) the offset adjustment input fibre.

Specification for transferring clock from pre-processor to digitiser (core): frequency variation, maximum jitter, mark-space ratio… This will be agreed between Sebastien Lhenoret and Jim Thornhill.

Protocol for global or broadcast commands over fibre, and broadcast commands from pre-processor to digitiser (core).
The protocol must include pulser control, core ADC offset and any commands sent via GTS which affect the digitiser. This will be agreed between Ian Lazarus and Sebastien Lhenoret

Protocol for fibre transferring CFD pulse from digitiser to pre-processing (core)
Sebastien Lhenoret and Ian Lazarus (including Jim Thornhill too?)

What to do with CFD pulse at the output from the pre-processing front panels
Issues include electrical isolation- whether to use opto-isolator- and also how to fan-in up to 180 signals to form the fast multiplicity of the Ge channels for use by the ancillary electronics. The second point is part of the ancillary detector group's work, but the isolation issue affects pre-processing too. Christophe Oziol will discuss this interface with Christophe Theisen.

Preamplifier Time Over Threshold (TOT) connections
We discussed the operation of the Time over Threshold method to measure pion energy. For the hardware connections we concluded that the inhibit signal will be transmitted from preamplifers to D15 in the digitiser data stream and into the pre-processing. No work needed on this interface.

Algorithm to recover from TOT in MWD
Lounis Benallegue and Cayetano Santos will make tests on their MWD implementations to see the effect of a large step input- Werner Gast told us that as long as we stop writes to the accumulator(s) during Inhibit (overload)- then we need just wait 1 MWD window before restarting.

Clock phase setup
Either of the 2 methods outlined by Marco Bellato in the earlier GTS presentation could be used. The repeated reset method needs no new hardware. The clock loop back method needs switches in the GTS mezzanines, but not in the other pre-processing mezzanines. The clock signal from pre-processing to digitiser is a synchronous fibre and the same clock will be reflected back on another fibre. The pre-processing core mezzanine will compare the difference in phase between the 2 clocks and report it to the GTS mezzanine.

The synch (also known as TOP) pulse will be sent from the GTS system to the GTS mezzanine in the pre-processor. From there it will be sent to the core mezzanine and the segment mezzanines. Then the core mezzanine will send the synch to the digitiser which will insert it in D15 of all data streams and send it back to the pre-processing mezzanines. Sync and Inhibit will be Or'ed into D15. During the startup calibration phase, the preamps will be prevented form sending Inhibit (for example by setting them to the mode where the over-range reset is triggered by the digitiser ADCs rather than from the internal discriminator in the preamps. During setup the ADC over-range bit could then be masked off to prevent preamp resets). Each mezzanine (core and segment) in the pre-processor will calculate the difference between the original GTS synch and the returned digitiser synchs.

The possibility of losing lock in the Rocket i/o links (GTS or digitiser to pre-processing) was raised. **It was agreed** that the action in this case should be to report the error to the run control software and to try to correct things locally if this can be done without affecting neighbouring channels. There was an open question as to the extent to the clock phase recalibration required after restarting a single link (with the consequent different latency). More work needed.

Werner Gast then raised the question of how we know that the system is running correctly in normal operation- how would we detect a missed (or extra) clock? The solution proposed was to periodically send the synch pulse from GTS and measure its return from the digitiser to pre-processor to see if anything has changed (by 1 clock). The pulse width of the D15 data line will easily distinguish the synch pulses from Inhibits since Inhibit will always be much wider than 1 or 2 clocks. However the synch cannot be seen whilst the preamplifier is sending Inhibit (note its unlikely that all segments

will send out an inhibit simultaneously, so the synch will be returned on at least some segments each time).

All these clock issues (setup/calibration, recovery after lost lock and periodic synchs) will be discussed and written up by a group comprising Patrick Coleman-Smith, Marco Bellato, Sebastien Lhenoret and Pierre Edelbruck.

Protocol & Interface summary table.

Green indicates fully defined signals (electrically and protocol); red shows partially defined signals for which protocol and/or hardware definitions are needed. Responsibilities were defined during the meeting and some overlap the lists above: overlaps are indicated by the use of initials rather than names.

Interface	Information and Protocol (if reqd)	Hardware	Who is Responsible?	Latest Document with full definition
Preamp core in/out	Charge Signal Control (Pulser…)	MDR 26, LVDS, analogue	Alberto, George & Patrice	Preamp spec 1.4
Preamp seg in/out	Charge Signal Control	MDR 26, LVDS, analogue	Alberto, George & Patrice	Preamp spec 1.4
Digitiser core data	Data stream (2)	2 Gbps fibre (2)	PCS, MB, SL, PE	Startup + online health check (new)
Digitiser seg data	Data stream (36)	2 Gbps fibre (6)	PCS, MB, SL, PE	Startup + online health check (new)
Pre-proc core clock/control/CFD	Offset control Clock, sync, CFD	2 Gbps fibre (2+4)	SL + JT/PCS/IL	Common Comms chap into dig & pp specs
Pre-proc seg control	Offset control	100Mbps fibre (1 per 6)	SL + JT/PCS/IL	Common Comms chap into dig & pp specs
Pre-proc - GTS	GTS internal Clock setup	2 Gbps fibres (2)	PCS, MB, SL, PE	Startup + online health check (new)
Pre-proc - PSA	To be discussed	ATCA CPU or switch output	Xavier, Marco Christophe	PP spec, PSA spec (new)

John Cresswell is also interested in the data format decisions which will form part of the pre-processing to PSA interface.

New documents to be produced:

- Startup procedures and online health checks.
- A common communications chapter for digitiser and pre-processing specifications.
- A common communications chapter for pre-processing and PSA (or DAQ?) specs.

Written by Ian Lazarus (3rd March 2005)